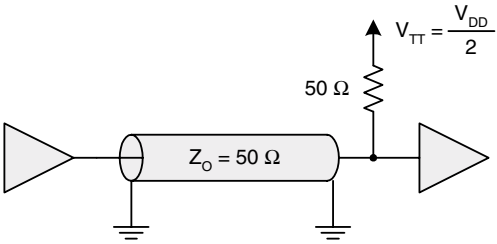

FIGURE 18.9 $V_{DD} \div 2$ termination.

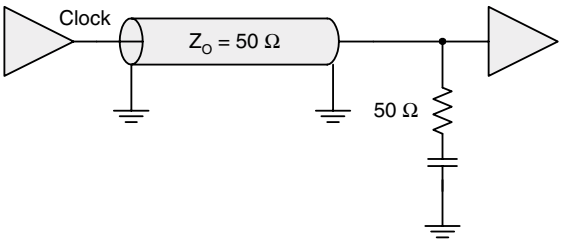

FIGURE 18.10 AC termination.

capacitor combines with a 50-Ω resistor to yield a time constant of 5 μs, which is suitable for most applications.

Some engineers do apply AC termination to normal unbalanced signals such as a data bus. The idea is to save power by presenting the termination resistor only during the high-frequency signal transition events and not during the longer static time. Smaller capacitors, perhaps 100 pF, are required in this case to provide low impedance at the high frequency edge but a low RC time constant so that it charges to the driven DC value quickly. Problems with this approach include added time for the wire to stabilize as a result of ringing and difficulty in matching the capacitor to the variation in driver's edge rate. AC termination may be the best solution for certain weak drivers with multiple loads, but some trial-and-error adjustment of the capacitor may be required in the lab.

Parallel termination can reduce power dissipation only to a point, because it is a shunt load to a DC voltage rail. Multidrop bus topologies require parallel termination, which prevents reflections from being formed at the transmission line ends. High-speed digital systems often employ point-to-point buses for reasons including source-synchronous clocking and transmission line stub reduction. Point-to-point buses also provide an advantage in not requiring parallel termination. *Series termination* can be used in these situations with its benefit of zero DC power dissipation. This technique was already briefly discussed in the context of clock distribution.

Series termination, also called *source termination*, operates by purposely creating a reflection at the load and then terminating that reflection at the source to prevent its re-reflection back to the load. A unidirectional point-to-point transmission line with series termination is shown in Fig. 18.11. When the driver first transitions, the transmission line presents its characteristic impedance as a load. In combination with the termination resistor, a voltage divider is formed, and only half the voltage propagates down the wire. When this half amplitude signal reaches the transmission line's unterminated end, a reflection coefficient of one causes the incident and reflected voltages to add with the result being the original full-amplitude signal. The receiving IC observes the full-amplitude signal.

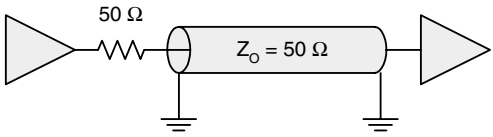

FIGURE 18.11 Series termination.

The reflected signal propagates back to the driver. This time, the transmission line end is terminated by the resistor connected to a power rail via the driver circuit itself, and the reflected energy is absorbed. There is no DC power dissipation with series termination, because the terminating resistor does not shunt the transmission line to a separate DC potential.

The reflection intentionally created in a series-terminated transmission line makes this scheme nonideal for high-speed multidrop buses, because it takes two round-trip times for the entire transmission line to stabilize. A 12"-in (0.3 m) bus would require approximately 4 ns for the transmission line to settle, which is a substantial fraction of the timing budget at speeds over 100 MHz.

Bidirectional point-to-point transmission lines can use series termination as well, with good results. Figure 18.12 shows a transmission line with series termination at each end. The mode of operation is the same as explained previously. When component A is driving, R1 serves as the series termination, and the signal propagates toward R2. R2 connects to the high-impedance input circuit at component B, effectively nullifying the presence of that resistor. A reflection is developed at the R2 end of the transmission line and is absorbed when it returns to the R1. Some delay and lowpass filtering of the signal may result because of the RC time constant formed by R2 and any stray capacitance at component B's input node. If the stray capacitance is up to 10 pF, the time constant is up to 500 ps—small, but non-negligible for very high-speed circuits.

Selecting the perfect series termination resistor is an elusive task, because it is difficult to characterize a driver circuit's actual output impedance. This finite impedance combines with the series resistor to yield the total termination impedance seen by the signal reflecting back from the load. A driver circuit's output impedance varies significantly with temperature, part-to-part variation, supply voltage, and the logic state that it is driving. It is therefore unrealistic to expect perfect series termination across time and multiple units manufactured. Some devices that are specifically designed for point-to-point transmission line topologies (e.g., certain low-skew clock buffers) contain internal series termination circuits that are designed to complement the driver's output impedance. In the remaining cases, standard resistance values are chosen with the understanding that an imperfect termination will result. A typical value of 39, 43, or 47 Ω can be chosen for an initial prototype build when using 50-Ω transmission lines, and the signal integrity can be evaluated in the laboratory. Switching to one of the other values may improve signal integrity by reducing the reflection coefficient.

Practically speaking, there is a common range for a driver's output impedance. If a 39 Ω termination resistor is chosen with the expectation that Z_{OUT} = 10 Ω, and the actual impedance under certain conditions is 3 Ω, the total termination will be just 42 Ω. For a 50 Ω transmission line, $|\Gamma| = 0.087$,

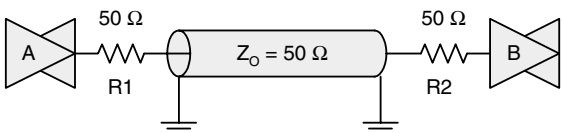

FIGURE 18.12 Bidirectional series termination.